WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first weight generator operative to receive a first sequence of phase values for a first analog signal and provide a first inphase weight and a first quadrature weight for each phase value in the first sequence;

a first signal generator operative to receive and multiply inphase and quadrature oscillator signals with first inphase and quadrature weights, respectively, and provide the first analog signal having a frequency and leading edges determined by the phase values in the first sequence; and

a digital clock generator operative to receive the first analog signal and generate a digital clock signal having a frequency determined by the frequency of the first analog signal.

2. The integrated circuit of claim 1, further comprising:

a second weight generator operative to receive a second sequence of phase values for a second analog signal and provide a second inphase weight and a second quadrature weight for each phase value in the second sequence; and

a second signal generator operative to receive and multiply the inphase and quadrature oscillator signals with second inphase and quadrature weights, respectively, and provide the second analog signal having leading edges determined by the phase values in the second sequence, and

wherein the digital clock generator is operative to generate a third analog signal having a leading edge for each leading edge in the first and second analog signals, and to generate the digital clock signal based on the third analog signal.

3. The integrated circuit of claim 1, further comprising:

a divider operative to divide the digital clock signal in frequency by an integer value of one or greater and provide an output clock signal having a frequency related to the frequency of the digital clock signal.

4. The integrated circuit of claim 1, further comprising:

a phase generator operative to generate the first sequence of phase values for the first analog signal based on a frequency control value.

5. The integrated circuit of claim 4, wherein the phase generator is further operative to generate the first sequence of phase values for the first analog signal based on a phase offset value.

6. The integrated circuit of claim 4, wherein the phase generator includes

a first accumulator operative to sum the frequency control value with a first accumulated value and provide a second accumulated value, and

a second accumulator operative to sum the frequency control value with the second accumulated value and provide the first accumulated value, and

wherein the first sequence of phase values is obtained from the first accumulator.

7. The integrated circuit of claim 6, wherein the first and second accumulators have at least sixteen bits of resolution.

8. The integrated circuit of claim 1, wherein the first signal generator includes

a first multiplier operative to multiply the inphase oscillator signal with the first inphase weights and provide a first intermediate signal,

a second multiplier operative to multiply the quadrature oscillator signal with the first quadrature weights and provide a second intermediate signal, and

a summer operative to sum the first and second intermediate signals and provide the first analog signal.

9. The integrated circuit of claim 8, wherein the first and second multipliers are implemented with four-quadrant multipliers.

10. The integrated circuit of claim 8, wherein the first and second multipliers are implemented with two-quadrant multipliers.

11. The integrated circuit of claim 1, wherein the first weight generator includes

a look-up table operative to receive the first sequence of phase values and provide a sine value and a cosine value for each phase value in the first sequence, and

a first digital-to-analog converter operative to receive the sine value for each phase value in the first sequence and provide the first quadrature weight for the phase value, and

a second digital-to-analog converter operative to receive the cosine value for each phase value in the first sequence and provide the first inphase weight for the phase value.

12. The integrated circuit of claim 11, wherein each phase value in the first sequence has at least eight bits of resolution and each sine value and each cosine value have at least six bits of resolution.

13. The integrated circuit of claim 1, further comprising:

an oscillator operative to provide the inphase and quadrature oscillator signals.

14. The integrated circuit of claim 13, wherein the oscillator is part of a phase-locked loop (PLL) and locked in frequency to a reference signal.

15. The integrated circuit of claim 13, wherein the oscillator is operative to provide the inphase and quadrature oscillator signals at a fixed frequency.

16. An apparatus comprising:

means for receiving a first sequence of phase values for a first analog signal and providing a first inphase weight and a first quadrature weight for each phase value in the first sequence;

means for multiplying inphase and quadrature oscillator signals with first inphase and quadrature weights, respectively, and providing the first analog signal having a frequency and leading edges determined by the phase values in the first sequence; and

means for receiving the first analog signal and generating a digital clock signal having a frequency determined by the frequency of the first analog signal.

17. The apparatus of claim 16, further comprising:

means for receiving a second sequence of phase values for a second analog signal and providing a second inphase weight and a second quadrature weight for each phase value in the second sequence;

means for multiplying the inphase and quadrature oscillator signals with second inphase and quadrature weights, respectively, and providing the second analog signal having leading edges determined by the phase values in the second sequence; and

means for generating a third analog signal having a leading edge for each leading edge in the first and second analog signals, and wherein the digital clock signal is generated based on the third analog signal.

18. An integrated circuit comprising:

a first weight generator operative to receive a first sequence of phase values for a first analog signal and provide a first inphase weight and a first quadrature weight for each phase value in the first sequence;

a second weight generator operative to receive a second sequence of phase values for a second analog signal and provide a second inphase weight and a second quadrature weight for each phase value in the second sequence;

a first signal generator operative to receive and multiply inphase and quadrature oscillator signals with first inphase and quadrature weights, respectively, and provide the first analog signal having a frequency and leading edges determined by the phase values in the first sequence;

a second signal generator operative to receive and multiply the inphase and quadrature oscillator signals with second inphase and quadrature weights, respectively, and provide the second analog signal having leading edges determined by the phase values in the second sequence and same frequency as the first analog signal; and

a digital clock generator operative to receive the first and second analog signals, generate a third analog signal having a leading edge for each leading edge in the first and second analog signals, and generate a digital clock signal having a frequency determined by the frequency of the first and second analog signals.

19. A clock generation system comprising:

an oscillator operative to provide inphase and quadrature oscillator signals having a fixed frequency;

at least one clock generator, each clock generator comprising

a first weight generator operative to receive a first sequence of phase values for a first analog signal and provide a first inphase weight and a first quadrature weight for each phase value in the first sequence,

a first signal generator operative to receive and multiply inphase and quadrature oscillator signals with first inphase and quadrature weights, respectively, and provide the first analog signal having a frequency and leading edges determined by the phase values in the first sequence, and

a digital clock generator operative to receive the first analog signal and generate a digital clock signal having a frequency determined by the frequency of the first analog signal.

20. The clock generation system of claim 19, wherein each clock generator further comprises

a second weight generator operative to receive a second sequence of phase values for a second analog signal and provide a second inphase weight and a second quadrature weight for each phase value in the second sequence, and

a second signal generator operative to receive and multiply the inphase and quadrature oscillator signals with second inphase and quadrature weights, respectively, and provide the second analog signal having leading edges determined by the phase values in the second sequence, and

wherein the digital clock generator is further operative to generate a third analog signal having a leading edge for each leading edge in the first and second analog signals and to generate the digital clock signal based on the third analog signal.

21. The clock generation system of claim 19, and comprising a plurality of clock generators, each clock generator generating a respective digital clock signal, and wherein the frequency of the digital clock signal for each clock generator is individually programmable.